

Integrating Active, Passive and EMI-Filter Functions in Power Electronics Systems: A Case Study of Some Technologies

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Abstract—Assemblies of power semiconductor switches and their associated drive circuits are at present available in modules. Upward into the multi-kilowatt range, mixed mode module construction is used. This incorporates monolithic, hybrid, surface mount, and wirebond technology. However, a close examination of the applications in motor drives and power supplies indicates that there has been no dramatic volume reduction of the subsystem. The power semiconductor modules have shrunk the power switching part of the converter, but the bulk of the subsystem volume still comprises the associated control, sensing, electromagnetic power passives (inductors, transformers, capacitors) and interconnects. This paper addresses the improvement of power processing technology through advanced integration of power electronics. The goal of a subsystem in a module necessitates this advanced integration, incorporating active switching stages, electromagnetic interference (EMI) filters, and electromagnetic power passives into modules by integration technology. The central philosophy of the technology development research in the National Science Foundation Engineering Research Center for Power Electronic Systems is to advance the state of the art by providing the concept of integrated power electronics modules (IPEMs) for all these functions. The technology underpinning such an IPEM approach is discussed.

Index Terms—Electromagnetic interference (EMI) filters, integrated power electronics modules (IPEMs).

I. INTRODUCTION

POWER electronic products, to date, are essentially custom-designed with a long design cycle time. The equipment is designed and manufactured using nonstandard parts. Manufacturing processes are labor intensive, resulting in high cost. Over the past decade, the performance of power electronics systems has been driven by improvement in semiconductor components. Moving from bipolar to MOSFET technology [1], [2], has resulted in switching time reduction that, to date, test the limit of structural inductances associated with packaging, as well as thermal handling. Thus, an order of magnitude increase

in switching speed, which is possible with new device technologies, will require substantial reduction in structural capacitances and inductances associated with device and system-level packaging.

In recent years, a level of integration has been developed where power semiconductors in die form are mounted on a common substrate and interconnected with wire bonding. Although miniaturization has been achieved to some extent, the number of interconnects and discrete functionalities of all components remain as in a converter based on discrete construction. In this approach, the possibilities for three-dimensional (3-D) integration are still limited, and electromagnetic layout constraints have become dominant. The thermal management in this type of packaging is essentially limited to one-dimensional heat removal from the die. It is perceived, however, that power electronics modules constitute one of the driving forces toward modularization and integration of power electronic systems. Recent innovations in power modules have been mostly driven by semiconductor development with the help of improved layout and packaging technologies [3].

While semiconductor devices will still be one of the drivers for future power electronics development, devices do not currently impose the fundamental limitation to power conversion technology. It has been argued for some time now that it is rather packaging, control, thermal management, and system integration issues that are the dominant technology barriers currently limiting the rapid growth of power conversion applications [4]–[7]. To address some of these issues, this paper briefly discusses the technology advancement needed to improve the characteristics of power electronics systems, as well as the technologies being developed for integration of multi-kilowatt power electronics. Among the technologies being developed, are planar metallization device interconnects, allowing 3-D integration of power devices, as well as the integration of power passives to increase the power density, as these dominate the physical size of the system. The technologies being developed will ultimately span a wide range of applications from distributed power systems to motor drives. This paper also discusses results obtained from the various technologies being developed within the research scope of the Center for Power Electronics Systems (CPES), whose mission is to promote an integrated approach to power electronics systems in the form of highly integrated power electronics modules (IPEMs). As these technologies result from the research program of CPES, it is

Manuscript received July 20, 2004; revised February 16, 2004. This work was supported by the ERC Program of the National Science Foundation under Award EEC-9731 677. Recommended by Associate Editor J.-L. Schanen.

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Digital Object Identifier 10.1109/TPEL.2005.846553

realized that they still essentially represent a laboratory scale approach.

CPES's vision is to develop an integrated system approach via power electronic modules (IPEMs) that can lead to a standardized power electronics systems approach which is suitable for automated manufacturing and mass production. The envisioned integrated power electronics solution is based on advanced integration concepts in the form of standard functional building blocks, namely, IPEMs, and the integration of these building blocks into application-specific system solutions. This approach will drive the development of standardized systems design via functional blocks, as well as the modularization and standardization of functional modules. The IPEM approach enables dramatic improvement in performance and cost-effectiveness of power electronic systems.

The impact of improvements in power electronics technology and system integration via the IPEM approach can be compared to the impact being realized by improvements in very-large-scale integrated (VLSI) circuit technology. Applications of VLSI technology have enabled rapid advances in information technology leading to the digital revolution, accompanied by a steady increase in standardization, modularization, functional integration, and a steady decrease in manufacturing costs of equipment. The IPEM approach will also enable increased levels of integration in the modules that comprise a power electronics system—devices, circuits, controls, sensors, and actuators—which can be integrated into manufacturable subassemblies and modules. The use of these modules/subassemblies will allow systems assembly for customized applications with relative ease—instead of having to design and build the systems from the component level. It is realized that the large variations in power levels for power electronics might initially confine the advantages of this approach to lower power levels and specific areas of application.

II. MOTIVATION FOR HIGH-DENSITY INTEGRATION

The advantages of incorporating high-density multi-functionality into solids through planar integration technology have been well illustrated by the advances of microelectronics in the past [8]. Although electronic energy processing is different from information processing, the following parallels are important to note:

- 1) both technologies have electromagnetics as a fundamental limit;
- 2) both technologies are eventually thermo-mechanically limited (i.e., in terms of interface failure modes and loss density);
- 3) both technologies are materials limited;
- 4) new applications for both are driven by a relentless downward cost spiral.

A. Technologies for Integration

Furthermore, present manufacturing processes of the different types of discrete components and their packaging as used in power electronics are not compatible with integration into one production line. Examples of these technologies are the power semiconductor processing, coil and transformer winding,

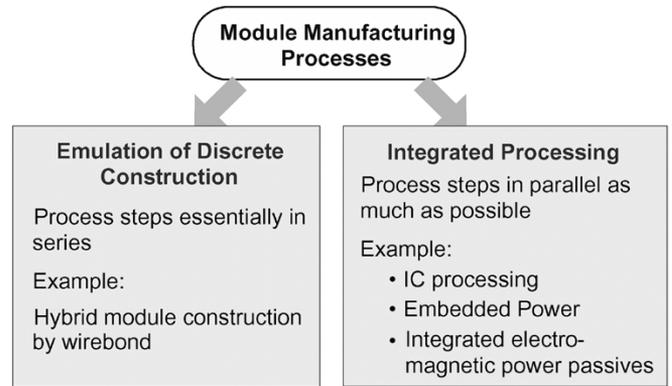


Fig. 1. Two types of module manufacturing processes, with the integrated processing showing process-level integration.

capacitor winding and other capacitor manufacturing methods, resistor manufacturing technologies, and the construction of power electronic converters in discrete component technology by wiring harness methods [9]–[11].

Compatible processes that can be incorporated into one integrated production line are needed. As the nature of the integrated module will be hybrid, however, it has to be assumed that there will be a materials based manufacturing process (for producing power semiconductor dies, magnetic sheets, dielectric sheets, substrate sheets, for example) preceding the planar metallization, the large area electrical and thermal contacting, the integrated planar power passive formation and the layer stacking and packaging operations [12]. We have developed our technologies with this approach in mind. To achieve this we have placed a limitation on the nature of the processes we use. Only the following processes are implemented in the technologies discussed further on, since they are all compatible with already existing manufacturing process for integrated modules:

- 1) planar metallization technology by sputtering and electroplating;
- 2) reflow soldering for high quality large area electrical-thermal interconnects;
- 3) low temperature sintering for high quality large area electrical-thermal interconnects;
- 4) photolithography and wet chemistry for pattern definition and etching;
- 5) plasma cleaning as intermediate process steps for interface improvement;
- 6) laser machining and trimming as mechanical formation steps;
- 7) encapsulation technology for electrical, mechanical, and thermal integrity.

The use of selections of these process steps will be found in each of the technologies described further in this paper.

As shown in Fig. 1, consideration should further be given to integration at the process technology level when developing the processes. Fig. 1 characterizes wirebonding as an essentially sequential interconnect/integration technology when applied to power electronic modules. As also shown in Fig. 1, it is desirable to achieve simultaneous execution of a large number of parallel steps when considering interconnection. Examples of this are

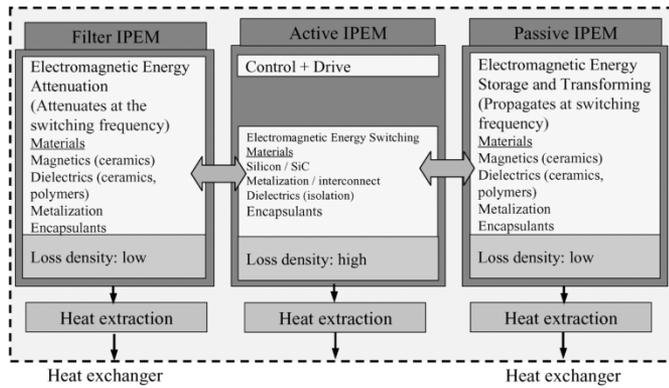


Fig. 2. Power electronics converter partitioning into active and passive IPEMs for optimum performance of integrated systems.

embedded power as a power switching stage integration technology and the integration of electromagnetic power passives as will be discussed in Section III of this paper.

B. Partitioning for Integration

Although the processes used in hybrid integration of electronic power processing have now been chosen to be compatible with an integrated production, it appears that other considerations dictate partitioning the integration of the system into different modules. As shown in Fig. 2, thermal and functional considerations favor the partitioning into active IPEMs for the power switching stages, passive IPEMs for the electromagnetic energy storage and conversion and filter IPEMs for the EMC. While the loss energy density in the switching devices is high, the loss energy density in the passive modules is low. This requires different thermal approaches for optimum module performance.

Furthermore, as will be discussed in Section III, the electromagnetic characteristics of the passive IPEMs are not suited to the integration of EMI filters when constructed according to the requirements for optimum module performance for storing and processing electromagnetic energy since the filter modules have to attenuate electromagnetic energy at the switching frequency and above. Consequently, a third type of IPEM for EMI filtering becomes necessary, also as based on functional considerations.

III. HIGH-DENSITY LOW-PROFILE INTEGRATED POWER ELECTRONICS STRUCTURES

As examples of achieving high-density power processing structures with potential for incorporation into 3-D integration in quasiplanar modules, the approaches discussed in this section were developed. These approaches use some or all of the process steps discussed in Section II to produce integrated active power switching modules and integrated electromagnetic power passive and filter modules for building integrated power electronic converters for currents up to 50 A and voltages up to 800 V.

A. Integrated Switching Modules in Embedded Power

“Embedded power (EP)” refers to an integration technology, which was developed in-house for packaging power electronics

switching (active) modules, incorporating multiple bare power chips, such as insulated gate bipolar transistors (IGBTs), MOS-FETs, and diodes, and associated components for drive, control, and protection [13]. The power chips are embedded in a 3-D, multilayer interconnect structure by sandwiching the power bus network and integrated circuitry. In addition, the planar metallization interconnection and use of a ceramic chip carrier lead to possibilities for functional integration, while planar integration processes such as photolithography, thin- and thick-films deposition, allow cost-effective automation during manufacture.

Used in the assembly of power electronics modules, most power semiconductor chips have an inherent vertical structure in which the metallization input/output (I/O) electrodes (pads) are arranged on two sides of the chips. Usually, the gate, source (or emitter) pads are located on the top surface with the thin film metal aluminum (Al) terminals and are ready for ultrasonic bonding. The drain (or collector) electrode is the deposited metallization (mostly Ag or Au) on the bottom of the chip, which is ready to be soldered to a base substrate. This vertical structure enables the building of a sandwich-type 3-D multichip module (MCM) construction. Fig. 3(a) conceptually illustrates the cross section view of a power electronics module designed in this way. It consists of three layers: 1) base substrate; 2) EP stage; and 3) components, connected by solder layers. In the structure, the EP stage—an integrated power chips component—is built on a flat ceramic frame, as shown in Fig. 3(b), with the chips embedded. The dielectric is used as an interlayer to protect the chip with defined vias on the top pads of the chips. The metallization is for the interconnection of multiple power chips through metallurgical contact to aluminum pads on the chips through vias in the dielectric layer; this replaces the bond wires in the conventional module, and is also used as the next-level interconnection for the attachment of associated components [layer 3 in Fig. 3(a)]. Layer 1, the base substrate, can be a direct-bond copper (DBC) ceramic substrate for the bottom solder interconnects of multiple chips and also offers a thermal downward path. After stacking three layers by soldering, the structure offers several advantages, such as sandwiched bus layout, closer component attachment, shorter interconnects, and a solid construction. This arrangement leads to higher power density, improved electrical performance and effective thermal dissipation. Fig. 3(c) shows the details of the pad contact, mounting and isolation. The original bare chips encompass the Al pads, the solderable bottom electrode and passivation layer outside the pad surfaces. An adhesive dielectric is used to affix the chips through filling the gaps between the chip edges and the openings in the ceramic frame. The bond layer is comprised of Ti and Cu thin-film layers, which provide good adhesion and low film stress, as well as excellent electrical/thermal conduction. For carrying high current, a thicker (>5 mils) Cu layer is deposited over the thin-film Cu layer.

The whole packaging process is designed as a two-step manufacturing operation: 1) the integration of multiple chips and 2) the 3-D assembly.

Fig. 4 illustrates the process flow of the embedded power chips stage. Step 1 involves the preparation of the ceramic frame (chips carrier), which is achieved by laser cutting a ceramic

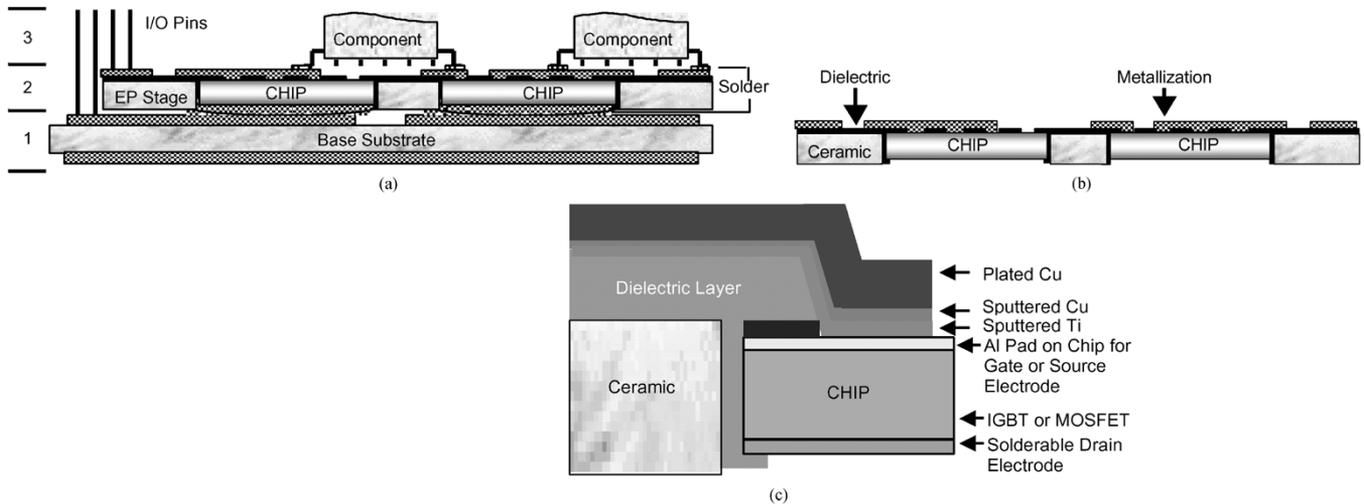


Fig. 3. (a) Structural schematic of an embedded power module, (b) an integrated power chips stage, and (c) chip mount, isolation, and pad contact.

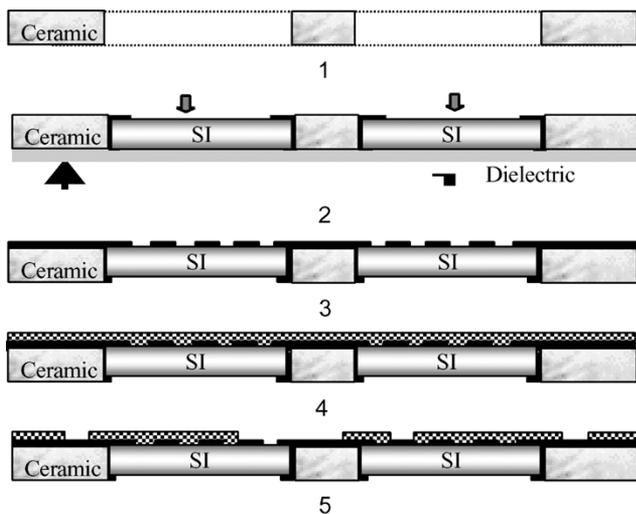


Fig. 4. Process steps of the embedded power chips stage.

plate. The openings formed are ready for the mounting of the power chips. For accurate alignment of the following processes, multiple tiny tips are formed around the edges of each opening to fix the chips tightly and to provide 500- μm -wide gaps. Step 2, mounting the chips, involves filling these gaps completely with a dielectric paste, then using temperature curing (150°C/7 mins). Now a flat substrate with co-planar chips is formed, which allows the subsequent planar processing. The whole surface is coated with a dielectric interlayer, as shown in Step 3, which defines the vias on the pads of the chips by using a screen-printing method with a prepared screen pattern. The screened dielectric paste also needs a curing of 200 °C/30 min to form a flat, good adhesive layer. Then, in Step 4, the metallization multilayers are deposited on the entire surface which forms contacts with the Al pads on the chips through via holes in the interlayer. Conventional sputtering is employed to deposit thin-film Ti and Cu layers. Electroplating is used to form a thicker Cu deposition. Finally, in Step 5, the metallization layer is patterned to form both the power and the control circuits as well as their I/O terminals.

B. Integrated Electromagnetic Power Passive Modules

In order to integrate the electromagnetic power passive components used in power electronic converters into modules, additional technology had to be innovated. This integration technology for power passives can best be described by first considering a simple bifilar spiral winding as shown in Fig. 5(a). This structure consists of two windings (A–C and B–D), separated by a dielectric material. This resultant structure has distributed inductance and capacitance and is an electromagnetically integrated LC-resonant structure for which equivalent circuit characteristics depend on the external connections [Fig. 5(a)]. Even more complex integrated structures can be realized by adding more winding layers. This has been demonstrated with an integrated resonant transformer structure (L–L–C–T) as shown in Fig. 5(b) and (c) [14]. The necessary process flow for realizing these integrated structures are shown in Fig. 5(d). Design of these structures requires deliberate increase and modification of naturally existing structural impedances to realize a particular equivalent circuit function—for example the increase of the intra-winding capacitance to form the LC resonant structure. The classical term “parasitics” therefore no longer applies and all the higher-order impedances are rather referred to as structural impedances. The spiral integrated power passive structure has been developed over a number of years with advances in electromagnetic modeling, design and loss determination [4], [5], [15]. Loss modeling now includes core losses, dielectric losses, and skin and proximity effects, and conduction losses for nonsinusoidal voltages and currents. The improved models have led to integrated structures with power densities in excess of 30 W/cm³ operated at frequencies of up to 1 MHz [16]. It has been shown elsewhere [18] that the power densities achievable with integrated electromagnetic power passives are at least double that achievable with discrete components.

This developed technology for integrated passive components has mostly been implemented in resonant converter applications [14]. However, its application in a nonresonant PWM converter has also been demonstrated [17]–[19], as will be outlined in the subsequent systems discussion in Section IV. In this application, the planar passive integration technology, together with the

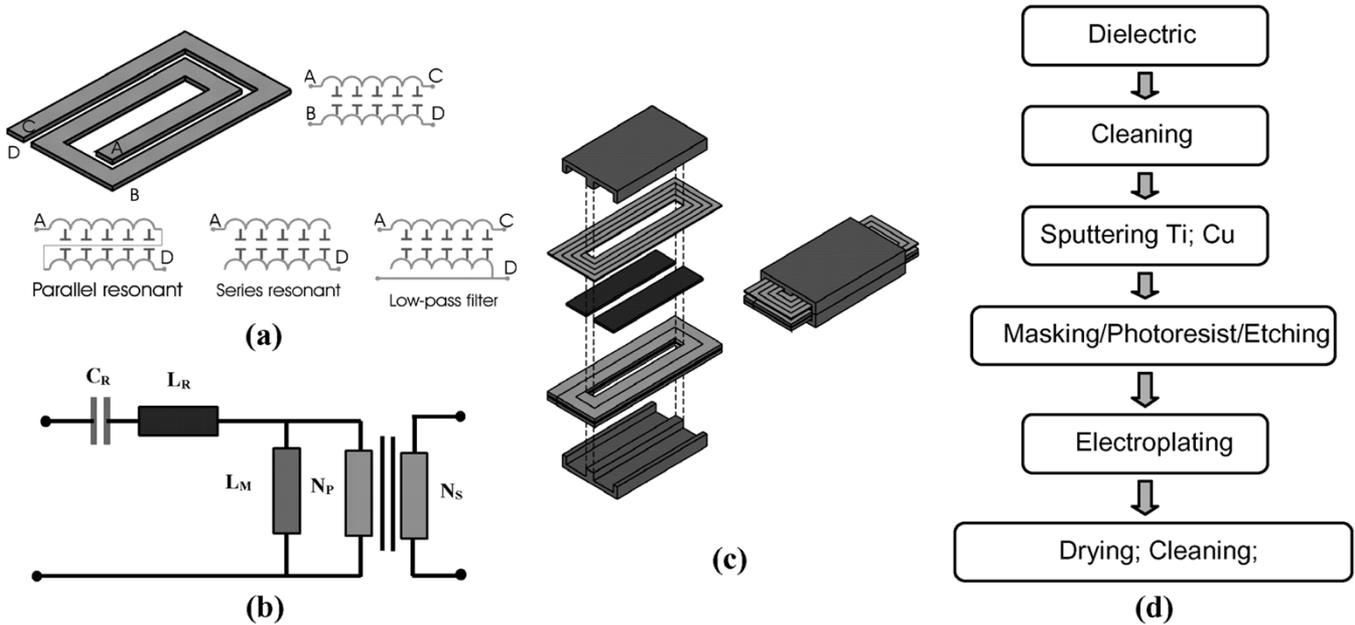


Fig. 5. (a) Spiral integrated LC structure with distributed capacitance and possible external connection configurations, (b) simplified equivalent circuit, (c) exploded view, and (d) process flow.

planar integrated magnetics technology were combined to integrate all of the high frequency passive components in a 1-kW asymmetrical half-bridge dc/dc converter (AHBC) for a distributed power system (DPS) application. The circuit diagram of the AHBC is shown in Fig. 13. The current-doubler inductors and the isolation transformer are not magnetically coupled, but can be integrated into two separate structures by splitting the isolation transformer and utilizing the equivalent magnetizing inductances to realize the current doubler inductors (reflected to the secondary). These two magnetic structures can in turn be integrated into one physical structure through integrated magnetics technology [17]. A cross section, reluctance diagram, and exploded view of this resultant first generation spiral integrated passive module are shown in Fig. 6. The I-core shares the flux for both of the integrated modules $LLCT_1$ and $LLCT_2$ and the ac flux is partially cancelled in the shared I-core as shown in Fig. 6(b). The relatively large dc decoupling capacitor is integrated into both the primary windings of the structure, using very high permittivity ($\epsilon_r > 12\,000$) ceramics [Fig. 6(c)].

C. Integrated EMI Filter IPEMs

In electronic power processing the switching function is used to control the flow of electromagnetic energy through the power processor. The switching function, however, is also the major mechanism of electromagnetic noise generation, which implies that a power electronics converter is potentially a large noise source to its vicinity. The increased switching frequency can to some extent, reduce converter size, weight, and cost, but will in turn increase EMI concerns. The advanced packaging and integration technologies also locate more components into smaller spaces. Consequently, circuit designers need to take much more care regarding electromagnetic interference (EMI). To reduce the cross talk among the power electronics converter and nearby equipment, much effort has been focused on improving circuit topologies to suppress switching noise by

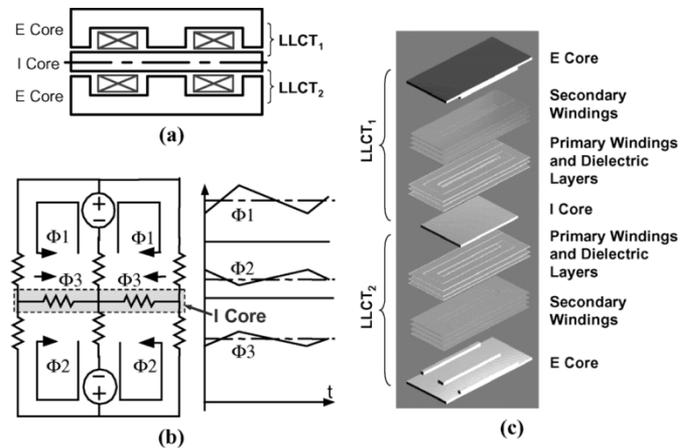


Fig. 6. (a) Cross section, (b) reluctance diagram, and (c) exploded view of nonresonant spiral integrated passive structure with integrated magnetics.

using soft-switching technologies, active and passive snubbers, so that the generated HF EMI noise at switching transient can be reduced. Recent work is more and more concentrated on developing advanced semiconductor devices with improved switching characteristics, such as wide band gap semiconductor devices. However, noise at switching frequency and its harmonics is inherent to the switching function of the power electronics converters; it can not be totally removed by the soft-switching techniques or advanced semiconductor devices. Therefore, EMI filters are always necessary.

Conventionally, EMI filters are implemented by using discrete components. The schematic of a typical EMI filter is shown in Fig. 7. Some problems for discrete EMI filters exist, however. First, because of the existence of the detrimental parasitic parameters of the discrete passive components, such as the equivalent parallel capacitance (EPC) of the common mode chokes and the equivalent series inductance (ESL) of

the capacitors, the effective filter frequency range is normally limited to a few megahertz. Second, the parasitic parameters caused by the filter layout will further affect the filters' high frequency performance detrimentally, so the EMI filter layout design always needs careful attention and it needs special expertise and experience. Third, the discrete EMI filter consists of a number of components. They must be processed differently and they are functionally and structurally separated. Each of the components is also packaged separately. This will increase use of material and manufacturing time. Finally, the different components of a discrete EMI filter have different type, value, size, and form factor, while interconnection space is necessary to connect all the components together. Hence, space normally can not be optimally utilized. In order to improve HF characteristics, shrink size, lower profile, and achieve structural, functional, and processing mechanical integration to reduce manufacturing time and cost, planar electromagnetic integration technology has been developed to integrate the EMI filters.

Integration of power electromagnetic components, such as high frequency transformers, resonant/choke inductors and resonant/blocking capacitors, for switch mode power supplies (SMPS) has been studied in order to reduce the count, volume, and profile of the components to increase the power density of the converter. Its applications in resonant and nonresonant SMPS have been reported [14]–[19]. However, very little work has been done on the subject of filter integration. To bridge this gap, the integration of an EMI filter for a DPS front-end converter was studied [20]. By applying the low-pass filter configuration of the planar Integrated L - C structure, as illustrated in Fig. 5(a), an EMI filter shown schematically in Fig. 7 can be integrated into a single planar module.

Although EMI filters also consist of electromagnetic passive components, their functions and requirements are different from that of other energy storage and transfer passive components in a power electronics converter. This is because EMI filters need to attenuate, instead of propagate, electromagnetic energy at switching frequency and above. Consequently, the high frequency characteristics, instead of efficiency, is the major concern for EMI filters. In order to improve high frequency characteristics of integrated EMI filters, specific technologies need to be developed, which include technologies to reduce EPC, reduce ESL, and increase HF losses.

To reduce the EPC of the integrated inductors, a narrow and thick conductor shape is more suitable than the conventional wide and thin conductor shape, which is normally preferable in other applications due to the requirement of reducing high frequency eddy current losses. For EMI filters, the narrow and thick conductor shape can reduce the conductor surface area, hence the structural winding capacitance can be reduced. It can also increase the high frequency eddy current winding losses to increase the high frequency damping factor [20]–[22].

To further reduce EPC, a staggered and interleaved winding structure is used. It greatly increases the distance between layers and greatly reduces EPC caused by magnetic coupling between CM choke windings, hence the structural winding capacitance can be appropriately reduced. By applying these technologies, the EPC of a constructed prototype is reduced from originally around 100 pF to less than 10 pF [21].

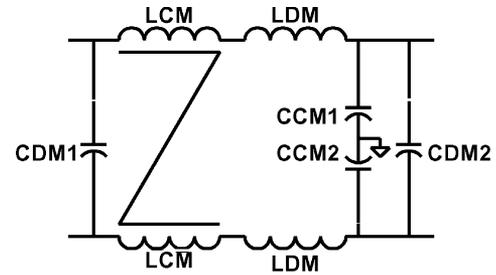


Fig. 7. Schematic of a typical EMI Filter.

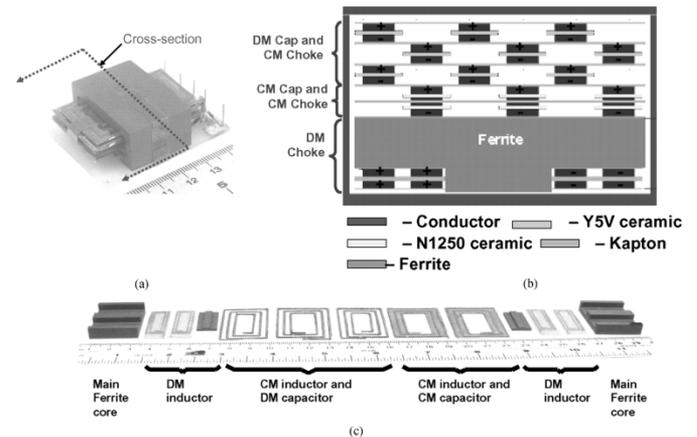


Fig. 8. Integrated EMI filter structure: (a) overview, (b) cross section view of half winding window, and (c) exploded view.

The ESL of the integrated capacitors can be reduced by using the transmission line connection method, since it shifts the ESL out of the capacitor branch [21]. To further increase the high frequency eddy current loss, multimetal metallization technology is introduced. Instead of using pure copper as the conductor material, a nickel–copper–nickel combination is used. Nickel is not only a higher resistivity material than copper, but its increased permeability gives a much smaller skin depth at the same frequency. Hence, the high-frequency eddy-current loss can be increased both for CM and DM noise current. The low frequency power current will automatically flow through the bulk copper layer, which will give low conduction loss and low temperature rise. The cross-section of an integrated EMI filter with staggered and interleaved spiral windings is shown in Fig. 8. Only half a winding window of the planar EE core is shown in Fig. 8 to illustrate the structure. The designed preliminary integrated EMI filter prototype has the same function as the discrete baseline filter, but higher power density, lower profile and similar or better HF attenuation. More detailed discussions on technologies and characteristics of integrated EMI filters can be found in [20] and [22].

Although EPC can be effectively reduced by using staggered and interleaved winding structures, the price to be paid is the greatly increased winding thickness and complexity. Furthermore, interleaving not only greatly reduces the stored electric field energy under CM excitation, but also greatly reduces the stored magnetic field energy under DM excitation. Consequently, the leakage inductance is greatly reduced and it will not be large enough to realize the required DM inductance.

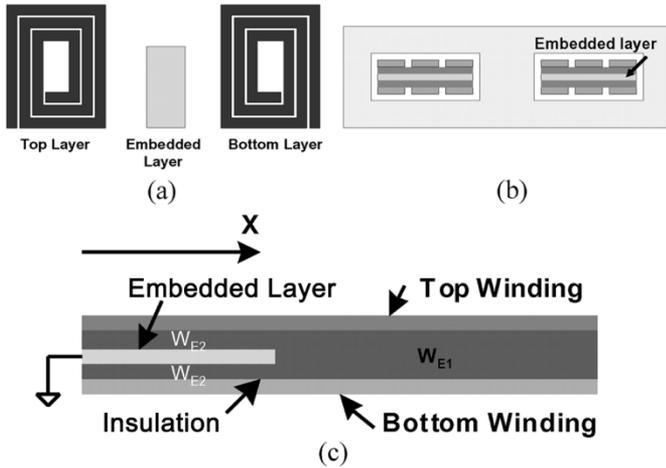


Fig. 9. Structure of windings with embedded conductive layer: (a) exploded view, (b) front view, and (c) side view.

Additional magnetic core and windings have to be inserted to implement the integrated DM inductor (shown in Fig. 8), resulting in compromised DM characteristics. As has been shown in [23], the EPC cancellation can be achieved by just simply embedding a grounded conductive layer between the planar CM choke windings, as shown in Fig. 9. After this grounded layer is embedded, the stored electric field energy is redistributed, divided into two parts: the energy stored in the space between choke winding layers (W_{E1}) and the energy stored in the space between windings and the embedded ground layer (W_{E2}) (shown in Fig. 9). As the area of the ground layer varies, the ratio of W_{E1} and W_{E2} also changes. It has been proved that when the embedded ground layer has a certain area so that $W_{E1} = W_{E2}$, the structural winding capacitance can be completely cancelled. The detailed equivalent circuit analysis can be found in [23]. In order to design the embedded layer, the energy based structural winding capacitance model for the planar spiral multilayer winding structures has been derived and the predicted results are within the acceptable accuracy range for design purposes [23]. The effectiveness of this technology has been demonstrated by a constructed $L-C$ low-pass filter with a planar inductor, in which a grounded conductive layer is embedded. The measured small signal transfer gain is shown in Fig. 10 and compared with the same inductor without the embedded layer. It is evident that with the embedded layer, the self-resonance caused by EPC is almost completely cancelled and much better high frequency attenuation can be achieved. This EPC cancellation technology can be applied to integrated EMI filters. Improved power density and improved high frequency characteristics can be accomplished [23].

IV. INTEGRATED POWER ELECTRONICS SYSTEMS: THE DPS EXAMPLE

A. DPS Implementation Using IPEMs: System-Level View

DPS are widely used in telecommunication and computer applications, and is the standard architecture for power distribution. Due to the power requirements of computer and telecommunication systems, the front-end ac-to-dc converter is the standard module for power delivery, which achieves PFC function

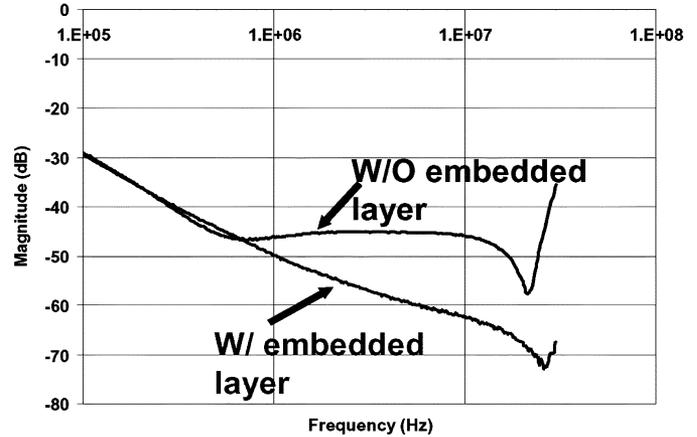


Fig. 10. Measured transfer gain of low-pass filter prototype.

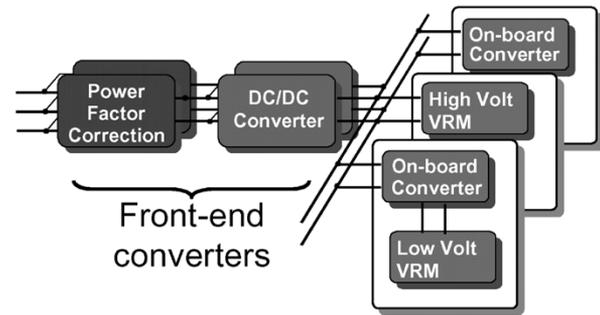


Fig. 11. Distributed power system.

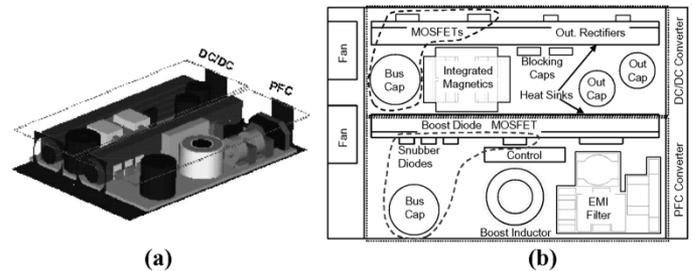


Fig. 12. Typical component layout for discrete DPS applications: (a) 3-D solid-body model and (b) top view and critical paths of a typical discrete DPS front-end converter.

and 48-V regulated output voltage. This standard power module has opened up the opportunity to develop a standardized modular approach to power processing, which will improve the design and manufacturing processes significantly, as well as enhance the electrical system performance. For this reason, a DPS front-end converter has been chosen to demonstrate the advantages of integrating power electronics systems, using a selection of the technologies described previously.

The structure of a typical DPS is shown in Fig. 11. In present industry applications, discrete devices are used to construct the whole DPS system, including the power stage, associated control, sensing, and gate drivers. A typical 3-D solid-body model representation for the front-end converter is shown in Fig. 12(a). Since the system construction requires discrete components, it is difficult to optimize space usage and to further increase the system power density. The solid-body model shows that the components of the front-end converter are distributed on the

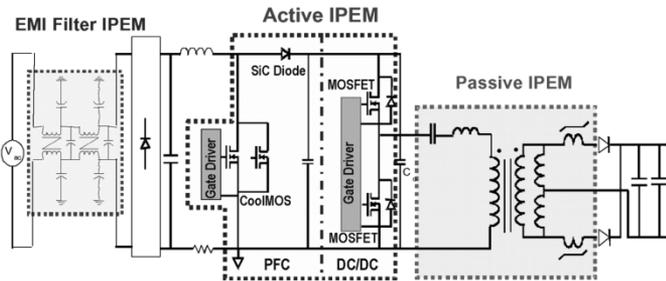


Fig. 13. DPS-System with EMI Filter IPEM, PFC front-end asymmetrical half-bridge dc/dc converter (AHBC) as active IPEM and passive IPEM.

printed circuit board, while copper traces are routed to distribute power and control signals to all devices. This layout approach presents severe limitations for both the electrical and the thermal aspects, as discussed elsewhere [18].

Fig. 12(b) shows the top view of the 3-D solid-body model. The major components of the converter are identified in the same figure, as well as the critical paths defining which components must be placed close to each other in order to reduce structural inductances. The inductance introduced by the copper trace to any of the critical loops will generate high voltage overshoot across the semiconductor devices during the switching period.

Locating the devices closer to each other will reduce the structural inductances. A clear limitation to this packaging approach lies in the space optimization, which is limited by the form factor of the various components. Therefore, the structural inductance of the packaging approach shown in Fig. 12(a) becomes a limiting factor to increasing the power level, switching frequency and consequently power density.

Although bringing devices together helps reduce the structural inductances, it is still limited by the structural inductances associated with the commercial packages. With discrete device technology, the minimum structural inductances that can be achieved are defined by the individual device packages. Although these are reduced, they still generate extra nonnegligible switching loss at high switching frequency. To further minimize the inductance of the critical paths, the only solution is by seeking integrated approaches for power devices and components.

The realization of an integrated power electronics system requires advances in technologies, which depend upon solutions to deal with the multi-disciplinary issues in materials, electromagnetic compatibility and thermal management.

The end objective is to integrate the functions and components for both the PFC and dc/dc converters shown in Fig. 11 in correspondence with the discussion on partitioning in II, Fig. 13 identifies the three blocks as an EMI filter IPEM, an active integrated power electronics module (active IPEM) and a passive integrated power electronics module (passive IPEM). The active IPEM represents the integration of power MOSFETs and gate drivers, for both the PFC and dc/dc stage. The main goals of the overall integration are to reduce the component count, increase power density, develop a modular approach, improve thermal management, and reduce the overall number of interconnections at the system level.

The starting point to designing an integrated system is to define specifications at the system and module levels. For this

TABLE I
DC/DC CONVERTER SPECIFICATIONS

Parameter	Specification
Input voltage	300 V – 415 V
Output voltage	48 V \pm 10%
Output voltage ripple (pk-pk)	480 mV
Isolation (output to ground)	>10k Ω
Output power	1 kW
Ambient temperature	50°C
Air flow at 5000ft	20 CFM at 50°C amb. 15 CFM at 35°C amb
Safety	UL 60950
EMI system-level	EN55022 Class B

TABLE II
ACTIVE IPEM REQUIREMENTS

Parameter	Specification
DC bus voltage (500V device)	400V
Surge of DC Bus voltage	415V
Power terminal current	25A
Junction temperature (max.)	150°C
Maximum operating junction temperature	125°C
Operating case temperature	-20°C -100°C
Isolation voltage (case-to-terminal at 60Hz)	>2500V
Power terminal leakage current	<500 μ A
Maximum switching frequency	500kHz

TABLE III
PASSIVE IPEM REQUIREMENTS

Parameter	Specification
DC blocking capacitance	>2 μ F
Leakage inductance (ZVS range 50%-100%)	2 μ H
Magnetizing inductance	45 μ H
Safety	UL 60950

reason, Table I shows the specifications for the dc/dc converter (system level) operated at 200 kHz, while Table II and Table III describe the requirements for the active and passive IPEMs (module level).

In the past, several approaches had already been developed by others for integrated packaging of power modules. Previous work reported a MCM-D package for power applications [24], where a Silicon chip with one power transistor was used as a MCM-D substrate onto which the gate driver was mounted using flip-chip technology. A high level of integration was accomplished, but the power bus was still interconnected to the base substrate using bond wires. This also occurred in the IPM packaging technology, where power chips were mounted and interconnected with bond wires onto a high-density substrate [25]. The concepts of embedded chips and bump-less bonding were also previously investigated for microelectronics packaging applications [26]. The planar device metallization technology that was developed in CPES and described previously, namely, embedded power [13], is a 3-D multilayer

integrated packaging technology that sandwiches power bus structure and integrated circuitry, and its implementation will be described subsequently.

B. Active IPEMs for the DPS

In the DPS front-end converter described previously, two power-switching stages were employed, respectively, in the PFC and dc/dc conversion parts [27]. These two switching stages are cascaded serially in the converter, as shown in Fig. 13, where the two stages comprise the active IPEM part. The stages operate at bus voltage of 400 V_{dc} and power rating of 1 kW.

The PFC stage (refer to Fig. 13) is designed for a single switch continuous-current-mode (CCM) converter. An advanced CoolMOSFET and SiC diode set, in a boost configuration, is chosen for switching at 400 kHz. This frequency ensures a good tradeoff between the size of the electromagnetic interference (EMI) filter, the boost inductor and the converter efficiency. For good thermal management, two parallel CoolMOSFETs and two parallel SiC diodes are adopted. A high-frequency bus capacitor is designed to decouple the possible parasitics of the external power connector. The maximum operational junction temperature is limited to less than $125\text{ }^{\circ}\text{C}$. The half-bridge power switching stage is designed for a 400-V/48-V dc/dc converter.

For high-density integration, the gate drive is assembled on a hybrid circuit with an Al_2O_3 substrate made by thick-film technology in this packaging version. The bare driver chips and components are surface mounted wire-bonded. This subassembly will be considered as a single component for the integrated embedded power stage.

1) *Integrated Power Chip Stages*: Fig. 14 presents the process series of the PFC stage manufacture. Four openings have been formed in a $625\text{-}\mu\text{m}$ -thick Al_2O_3 ceramic plate by laser machining [Fig. 14(a)]. Two large openings, each with eight tiny tips around, are for the mounting of MOSFETs, and the two small ones are for the SiC diodes. The gap width between the edges of the chip and the edges of the opening is 0.5 mm. It is filled by dielectric paste to affix the chips in the openings [Fig. 14(b)]. The curing of the dielectric is performed in an oven for seven minutes at $150\text{ }^{\circ}\text{C}$. The tips ensure that the chips are located in the accurate positions. After screen-printing and curing ($200\text{ }^{\circ}\text{C}/30\text{ min}$) of the dielectric paste, six via holes are formed on the source pad, and one on the gate pad of each MOSFET chip. The source hole is a 1-mm-diameter circle, and the gate hole is a 0.3-mm^2 . A 1-mm-diameter circular hole is also formed on top of each diode chip. Then, the metallization layer is deposited on the surface and etched with the designed pattern [Fig. 14(c)], which forms a large CoolMOS source and diode anode on the top of the ceramic frame, as well as the wiring circuit for the attachment of the gate drive circuit, bus capacitor, and input pins. On the backside, the CoolMOS drains and diode cathodes of the chips are directly exposed for soldering interconnection to the substrate [Fig. 14(d)]. The ceramic frame-based stage incorporates all PFC power chips and the planar interconnect circuit. Its size is $28.45 \times 23.12\text{ mm}^2$.

Performing the same process steps, the two MOSFET chips for the dc/dc converters (see Fig. 13) are integrated in an

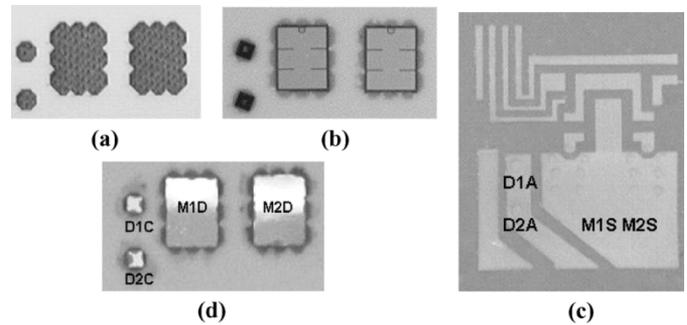


Fig. 14. Fabrication process for the integrated multichip embedded power stage: (a) ceramic frame, (b) chip mount, (c) metallization pattern on the topside, and (d) backside view of the stage.

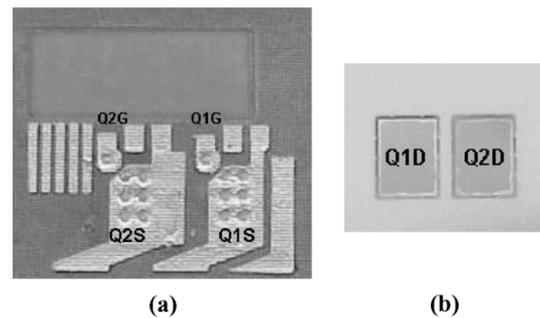


Fig. 15. Fabrication for the dc/dc integrated multichip stage: (a) topside metallization and (b) backside-chip bottom metallization.

identical Al_2O_3 ceramic frame, as shown in Fig. 15. Its size measures $28.45 \times 27.32\text{ mm}^2$. The top metallization pattern [Fig. 15(a)] includes large source electrodes and small gate single input electrodes, as well as the bus capacitor trace and the input signal pin traces. The signal and power terminals around the MOSFET are physically separated. The drain electrodes on the chip bottoms are exposed. As subassemblies, the stages are ready for the next level assembly.

2) *Assembly of a Subsystem IPEM*: The power chips stages can be further connected on both surfaces by soldering. The associated components can be mounted onto the top metallization. Fig. 16(a) shows that the bus capacitor, components for gate drive, and input pins are mounted onto the top metallization of the PFC stage. Fig. 16(b) shows that the gate-drive hybrid circuit board, bus capacitor, and input signal pins are mounted onto the top metallization pattern of the dc/dc stage. For the backside stacking interconnection, an Al_2O_3 DBC substrate of $28.45 \times 50.44\text{ mm}^2$ is patterned on the topside with compact traces for each chip electrode, as shown in Fig. 16(c). The bottom side is entirely soldered onto a heat spreader made of Cu plate. The Cu posts are mounted on the top traces and form the power terminals.

When the dc/dc and PFC sub-assemblies shown in Fig. 16(a) and (b) are soldered on the top surface of the DBC substrate, a stacked MCM has been constructed. Fig. 16(d) shows such a 3-D IPEM module encapsulated in a plastic case with silicon gel. The power terminals finally connect the metallization traces on top of the DBC substrate and on top of the chip stages, which are connected with the electrodes of the chips. The module shows the top pins as electrical input and output

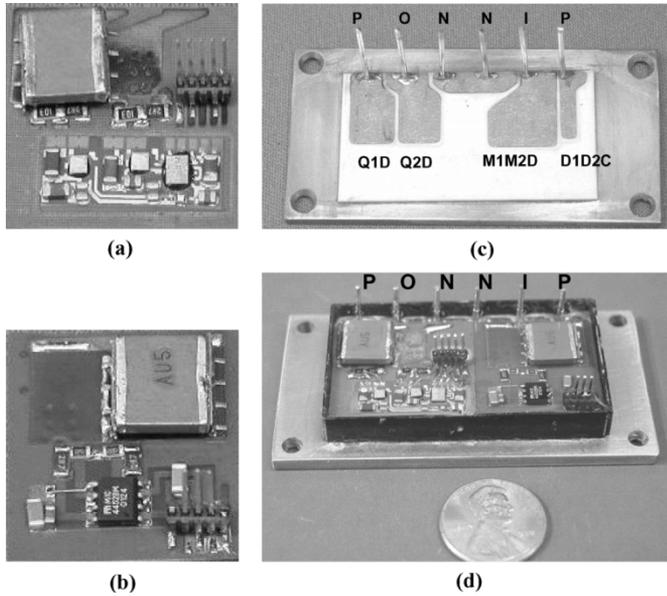


Fig. 16. IPEM assembly from the integrated chip stages: (a) associated components mounted on the top metallization of dc/dc stage, (b) associated components mounted on the top metallization of PFC stage, (c) patterned DBC base substrate attached on a Cu heat spreader plate, and (d) a full PFC + dc/dc IPEM mounted on the base substrate and encapsulated.

terminals and the bottom Cu plate as the thermal management interface.

3) *Electrical Characterization*: The electrical performance of the module was experimentally evaluated. The static characteristics of the power devices in the modules included insulation capability and contact resistance of the metallization interconnection. The switching performance was detailed because of its strong dependence on the parasitics of the packaging structure. The measurements of PFC and dc/dc IPEMs were both carried out. For the PFC part, a testbed was set up in the configuration of a complete boost converter.

Fig. 17 illustrates the efficiency comparison of the PFC IPEM and a similar discrete PFC. At an input voltage ranging from 150 to 250 V ac, the IPEM version increases the converter efficiency by 0.5%–1.2%, illustrating the improved switching and conduction performance.

The measurements of the dc/dc IPEM were carried out, using a setup with LC loads, at 400-V dc bias and 12-A peak current (in inductance), with $f_s = 200$ kHz, $t_r = 23.6$ ns, and $t_f = 24.4$ ns. For comparison, the wirebond and the EP modules were measured under the same conditions.

Maxwell Q3D parameter extractor, based on the partial element equivalent circuit (PEEC) method, was utilized to obtain the electromagnetic parasitics. The details of this method have been described in other work [28]. Table IV lists the dc/dc IPEMs main parasitic parameters and the comparison to a typical wirebond module. L_D and L_S represent the structural inductance corresponding to the drain and source interconnections, respectively. They are connected in series in the power path and greatly affect the power switching process. The structural inductance of the IPEM has 25% of the value compared to the wire-bond interconnect. The parasitic capacitors between the terminals (Pins P, O, and N in Fig. 16) and the ground

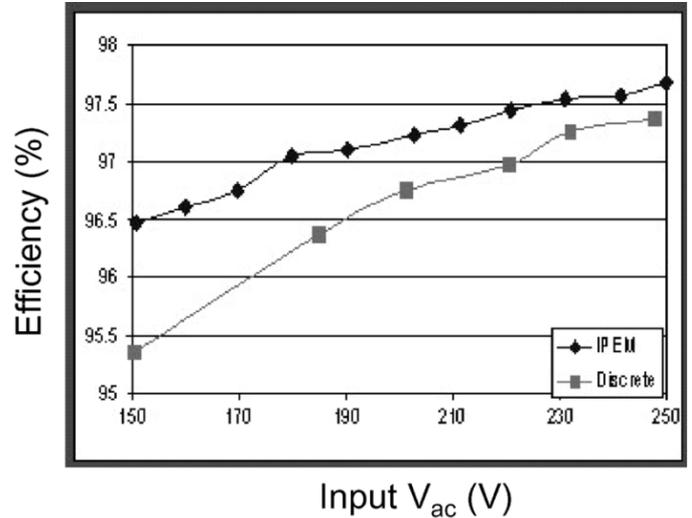


Fig. 17. Efficiency comparison of the PFC converters.

TABLE IV
MAIN PARAMETERS IN dc/dc IPEM COMPARED TO A DISCRETE VERSION

Parameters	Discrete	IPEM
Turns ration of transformer	8:3	4:3
Magnetizing inductance of T (μH)	45	N/A
Filter inductance (μH)	85	N/A
Magnetizing inductance of T1 (μH)	N/A	43.8
Magnetizing inductance of T2 (μH)	N/A	44.0
Resonant inductance (μH)	2.0	1.8
DC blocking capacitance (μF)	2.04	2.5
Profile (cm)	4.4	1.6
No. of passive components	6	1
Volume of components (cm^3)	173	82
No. of terminals	15	5
Volume of interconnections (cm^3)	170	5
Total volume (cm^3)	343	87

will affect the system's EMI performance. In addition, the turn-off loss of the IPEM shows reduction from 48 to 25 μJ under the conditions cited above. The footprint is reduced by 47%. The thermal dissipation capability is improved from 5 to 9 W/cm^3 for the same temperature rise.

C. Design and Implementation of Passive IPEMs in the DPS

For the design of the second generation passive IPEM, constraints and parameters for all components were obtained from the system requirements and circuit analyses, as illustrated in Table IV.

Because of the current doubler configuration, the structure of the passive IPEM was now realized by stacking two transformers and using only one dc blocking capacitor, as illustrated in Fig. 18(a). The transformers are built with two planar E-cores

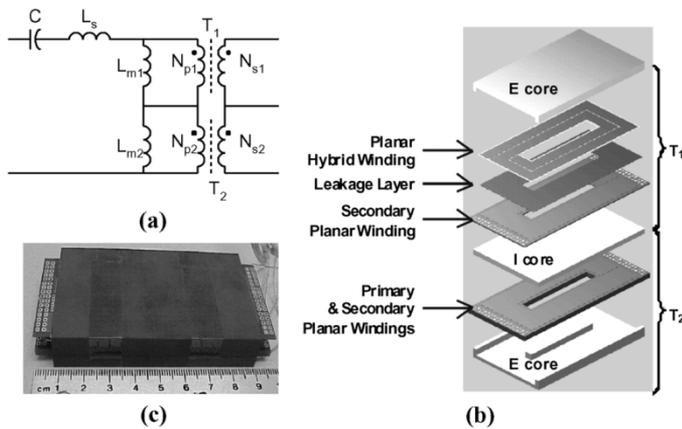


Fig. 18. Components of the passive IPEM: (a) equivalent circuit, (b) exploded view of the passive IPEM, and (c) 1-kW prototype.

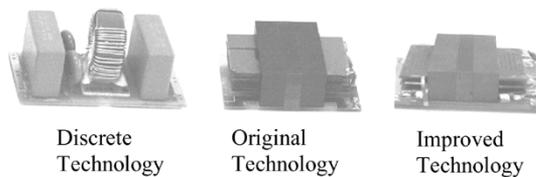


Fig. 19. Comparison of discrete and integrated EMI filter prototypes.

that share a common I-core, as detailed in Fig. 18(b). The dc blocking capacitor of the AHBC is now implemented in only transformer T_1 using the hybrid winding technology [17], [29]. This technology is implemented using Cu traces on both sides of the winding and a dielectric layer placed in the middle to enhance the capacitive component of that winding. The transformer T_2 is a conventional planar low-profile transformer. As already mentioned, the inductances of the current doubler output filter are realized by the magnetizing inductances of both transformers. Fig. 18(c) shows a picture of the final generation 2 passive IPEM implemented for the AHBC.

D. EMI Filter IPEM for DPS

Applying the integration and EPC cancellation technologies for integrated EMI filters, an improved integrated EMI filter prototype with structural winding capacitance cancellation for DPS was designed and constructed, as shown in Fig. 19. The processing steps are following the technologies outlined in Section II. To evaluate its performance, a baseline discrete EMI filter with the same component values is also constructed. The parameters comparison of the improved EMI filter, the previous developed integrated EMI filter without embedded layer and the baseline discrete filter is shown in Table V. The CM and DM small signal transfer gains for the filter were measured by using an HP 4194 A impedance/gain-phase analyzer. The measured characteristics are shown in Fig. 20. From these measurement results, it can be concluded that the integrated EMI filters have the same function as the discrete versions, but with structural, functional and processing integration achieved. The improved integrated EMI filter has about half the total volume and profile as the discrete filter, but much better high frequency DM characteristics and similar high frequency CM characteristics. Further

TABLE V
PARAMETERS COMPARISONS FOR INTEGRATED EMI FILTERS

Parameters	Discrete	Previous integrated	Improved integrated
LCM (mH)	3.3	3.1	4.5
LDM (μ H)	16.7	21	21
CCM (nF)	3.3×2	3×2	3.3×2
CDM (μ F)	0.68×2	0.7×2	0.7×2
EPC (pF)	12	17	N/A
ESL (nH)	70	30	< 10
No. of Comp.	5	1	1
Profile (cm)	2.6	1.6	1.2
Volume (cm^3)	39.8	27.4	20

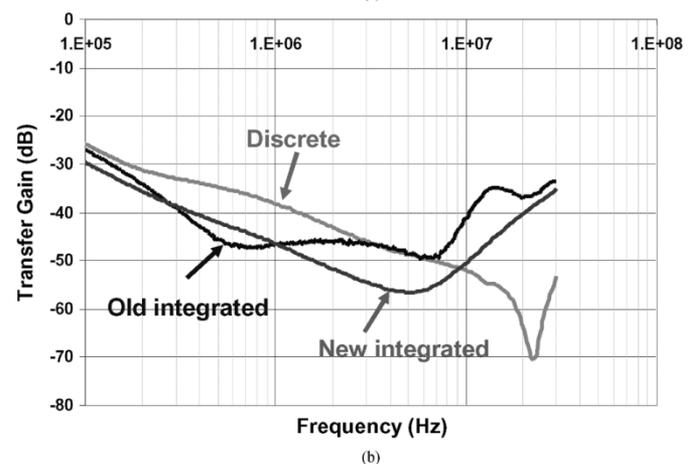
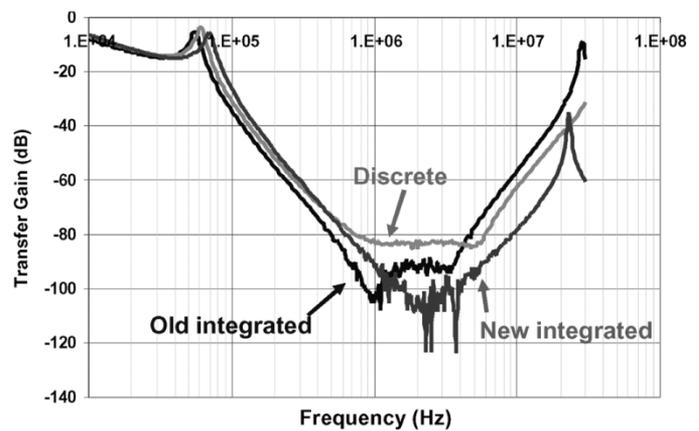


Fig. 20. Measured transfer gain comparisons: (a) DM transfer gains and (b) CM transfer gains.

improvement on CM performance is being researched and the progress will be reported in future publications.

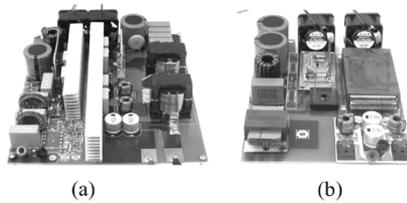


Fig. 21. Comparison of the hardware of discrete and integrated DPS system: (a) discrete devices DPS and (b) IPEM-based DPS.

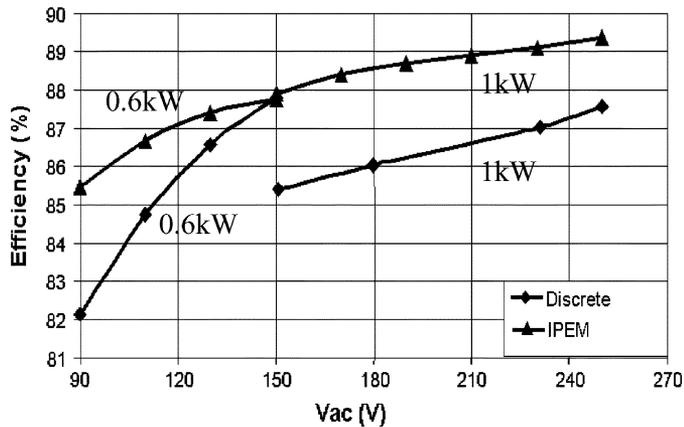


Fig. 22. Efficiency comparison between IPEM and discrete approaches for DPS front-end converters.

E. Integrated DPS Converter

To demonstrate the benefits of the IPEM concept at the system level, two 1-kW front-end ac/dc converters were built using exactly the same topologies, one using discrete devices and the other one using IPEMs. As shown in Fig. 13, the system is constructed in two stages: PFC and dc/dc stages. For the PFC stage, a 400-kHz single switch PFC using CoolMOS and SiC diode were chosen to achieve a smaller boost inductor and smaller EMI filter size. The asymmetrical half bridge operating at 200 kHz was used for the dc/dc stage, since the primary side switches can easily achieve ZVS. The converters are designed for a universal input of 90–264 V, and will derate below 150 to 600 W. The hardware for the two converters is shown in Fig. 21.

By using integration, the density and the form factor of the active and passive devices are appreciably improved. Consequently, the system level power density of the converter improved dramatically. For the discrete approach, the power density was 7.5 W/in³, while for the IPEM-based converter, the power density can be as high as 11.4 W/in³ with still much room for improvement.

By replacing the discrete active and passive devices, by IPEM sub-assemblies, the whole system only consists of a few modules, which is well suited to automated assembly. Not only has the system structure been improved, but the system electrical performance has been improved as well. As shown in Fig. 22, the system efficiency increases more than 2% at the high line voltage range, and more than 3% at 90 V, simply by using the active and passive IPEMs. Since the conduction loss of the active

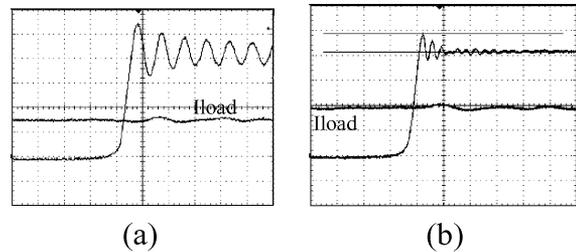


Fig. 23. Voltage overshoot comparison PFC and IPEM based PFC: (a) discrete and (b) IPEM, 100 V/div, 5 A/div, 20 nS/div.

IPEM is approximately the same for the same operating conditions, the major improvement is in switching loss reduction by minimizing the structural inductances.

At the same time, due to the smaller structural inductance in the critical path of the converter, less voltage stress on the devices occurs. For the discrete PFC switch, with turn off current 7 A, the voltage overshoot is 123 V. But with an active IPEM, turn off at the higher current of 10 A, results in a voltage stress of only 72 V, as shown in Fig. 23.

V. CONCLUSION

In the past, advances in semiconductor technologies have been the major driving force for reducing power electronics converter size, weight, and cost—mostly due to an increase in switching frequency. This increase in frequency and reduction in size have led to an increase in electromagnetic and thermal coupling in the physical system. Consequently, an order of magnitude increase in switching frequency will require substantial reduction in structural inductances associated with device and system-level packaging, as well as require improved thermal characteristics. Therefore, to further improve performance, reliability, and reduce cost, it is essential to develop novel integration and packaging technologies in the form of IPEMs, which must enable the integration of all the converter functions and not only concentrate on the switching stage.

These novel integration and packaging technologies, in conjunction with suitable devices, sensors and integrated design tools used to exploit the physical properties of available materials have been the research focus of the Center for Power Electronics Systems. This paper has discussed some of these integration and packaging technologies and illustrated their advantages. The role of the technologies mentioned above in the IPEM concept is key to achieving high levels of integration and to enable significant growth of the power electronics industry. It is evident that further innovations will be necessary as power densities increase. The impacts of system integration via IPEMs will enable a rapid growth of power electronics applications with reduced costs and design cycles that can be compared to the impacts in computer applications brought up by the VLSI circuit technology. The use of these technologies will also introduce different failure modes at the module level [30]–[32] and require changes at the systems level regarding maintenance, testability and reliability. These issues could not be addressed in this paper.

ACKNOWLEDGMENT

The authors would like to thank Dr. J. T. Strydom, Dr. W. Dong, D. Huff, Dr. L. Zhao, Dr. Z. Chen, Y. Pang, and E. Sewall, for their contributions to this paper.

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